What is claimed is:

1. A method of processing pixel levels, the method comprising:

clamping a pixel readout line to a voltage level less than a voltage corresponding to a pixel signal;

subsequently coupling the pixel readout line to an output of an n-MOS source-follower and reading out the pixel signal onto the pixel readout line through the n-MOS source-follower; and

storing a signal corresponding to the pixel signal that was read out.

2. The method of claim 1 wherein clamping the pixel readout line includes discharging a capacitance on the pixel readout line.

3. The method of claim 2 wherein discharging the pixel readout line is performed while processing a previously-stored pixel signal.

4. The method of claim 2 wherein discharging the pixel readout line includes disabling a pixel selection switch.

5. The method of claim 2 wherein discharging the pixel readout line includes enabling a switch to couple the pixel readout line to ground.

6. The method of claim 1 including:

clamping a capacitive storage node in a pixel signal processing circuit to a voltage less than a voltage corresponding to the pixel signal appearing on the pixel readout line;

subsequently coupling the pixel readout line to the storage node in the processing circuit; and

storing the signal corresponding to the pixel signal on the capacitive storage node.

8. The method of claim 7 wherein the storage node is clamped to substantially the same voltage and at about the same time as the pixel readout line.

9. The method of claim 7 including:

resetting the pixel;

subsequently reading out a reset signal through the n-MOS source-follower; and

storing on a second capacitive storage node in the processing circuit a signal that corresponds to the reset signal.

10. The method of claim 9 including:

prior to storing the signal corresponding to the reset signal, clamping the second capacitive storage node to a voltage less than the voltage corresponding to the reset signal; and

subsequently coupling the pixel readout line to the second storage node to store the signal corresponding to the reset signal on the second storage node.

11. The method of claim 1 including passing the pixel signal that was read out through a p-MOS source-follower.

12. The method of claim 11 including:

clamping a capacitive storage node in a pixel signal processing circuit to a voltage greater than the pixel signal appearing at an input to the p-MOS source-follower, wherein the storage node is clamped before passing the pixel signal through the p-MOS source-follower to the processing circuit; and

subsequently coupling an output of the p-MOS source-follower to the storage node in the processing circuit.

13. The method of claim 12 including:

resetting the pixel after storing the signal corresponding to the pixel signal in the processing circuit;

subsequently reading out a reset signal through the n-MOS source-follower;

passing the reset signal through the p-MOS source-follower to the processing circuit; and

storing a signal corresponding to the reset signal in the processing circuit.

14. The method of claim 13 wherein, prior to passing the reset signal through the p-MOS source-follower, a second capacitive storage node in the processing circuit is clamped to a voltage level higher than the reset signal appearing at the input to the p-MOS source-follower.

15. The method of claim 13 including converting a difference between the pixel and reset signals stored by the processing circuit to a corresponding set of digital signals.

16. An imager comprising:

a pixel readout line;

an active pixel sensor including an n-MOS source-follower through which signals sensed by the sensor can be read out to the pixel readout line, a first switch that can be enabled to read out signals from the sensor, and a reset switch;

a signal processing circuit that can be coupled to the pixel readout line; and

a controller configured to provide control signals to cause the pixel readout line to be clamped to a voltage level less than a voltage corresponding to a signal sensed by the sensor, and subsequently to cause the sensor signal to be read out through the n-MOS source-follower to the pixel readout line and to be stored by the processing circuit.

17. The imager of claim 16 wherein the controller is configured to provide a control signal to cause the first switch to be disabled while a previously-stored sensor signal is being processed by the processing circuit.

18. The imager of claim 16 including a third switch coupled between the pixel readout line and ground, wherein the controller is configured provide a control signal to cause the pixel readout line to be clamped by enabling the third switch.

19. The imager of claim 16 wherein the processing circuit includes a capacitive storage node, and wherein the controller is configured to provide control signals to cause the capacitive storage node to be clamped to a voltage less than a voltage corresponding to the sensor signal appearing on the pixel readout line, and subsequently to cause the pixel readout line to be coupled to the storage node.

20. The imager of claim 19 wherein the storage node is clamped to substantially the same voltage and at about the same time as the pixel readout line.

21. The imager of claim 19 wherein the processing circuit includes a second capacitive storage node, and wherein the controller is configured to provide control signals to cause the reset switch in the pixel to be enabled, and subsequently to cause a reset signal to be read out onto the pixel readout line through the n-MOS source-follower, and to cause a signal that corresponds to the reset signal to be stored on the second capacitive storage node.

22. An imager comprising:

a pixel readout line;

an active pixel sensor including an n-MOS source-follower through which signals sensed by the sensor can be read out to

the pixel readout line, a first switch that can be enabled to read out signals from the sensor, and a reset switch;

a signal processing circuit;

a p-MOS source-follower having an output that can be coupled to the processing circuit; and

a controller configured to provide control signals to cause the pixel readout line to be clamped to a voltage level less than a voltage corresponding to a signal sensed by the sensor, and subsequently to cause the sensor signal to be read out through the n-MOS source-follower to the pixel readout line and to be passed to the processing circuit through the p-MOS source-follower.

23. The imager of claim 22 wherein the controller is configured to provide a control signal to cause a capacitive storage node in the processing circuit to be clamped to a voltage greater than the sensor signal at an input to the p-MOS source-follower, wherein the storage node is clamped before passing the sensor signal through the p-MOS source-follower to the processing circuit, and wherein the controller is configured to provide a control signal to cause an output of the p-MOS source-follower subsequently to be coupled to the storage node in the processing circuit.

24. The imager of claim 23 wherein the processing circuit includes a switch that is coupled to the storage node and that selectively can be closed to clamp the storage node to the voltage greater than the sensor signal, and wherein the controller is configured to provide a control signal to cause the switch in the processing circuit to be temporarily closed before causing the output of the p-MOS source-follower to be coupled to the storage node.

25. The imager of claim 23 wherein, when the output of the p-MOS source-follower is coupled to the storage node, the

processing circuit stores a signal corresponding to the sensor signal, and wherein the controller is configured to provide control signals to cause the reset switch subsequently to be enabled, and to cause a reset signal to be read out from the sensor through the n-MOS source-follower and passed through the p-MOS source-follower to the processing circuit such that the processing circuit stores a signal corresponding to the reset signal on a second capacitive storage node.

26. A method of processing pixel levels, the method comprising:

clamping a pixel readout line to a voltage level greater than a voltage corresponding to a pixel signal;

subsequently coupling the pixel readout line to an output of a p-MOS source-follower and reading out the pixel signal onto the pixel readout line through the p-MOS source-follower; and

storing a signal corresponding to the pixel signal that was read out.

27. The method of claim 26 wherein clamping the pixel readout line is performed while processing a previously-stored pixel signal.

28. The method of claim 26 including:

clamping a capacitive storage node in a pixel signal processing circuit to a voltage greater than a voltage corresponding to the pixel signal appearing on the pixel readout line;

subsequently coupling the pixel readout line to the storage node in the processing circuit; and

storing the signal corresponding to the pixel signal on the capacitive storage node.

29. The method of claim 28 wherein the storage node is clamped to substantially the same voltage and at about the

same time as the pixel readout line.

30. The method of claim 28 including:

resetting the pixel;

subsequently reading out a reset signal through the p-MOS source-follower; and

storing on a second capacitive storage node in the processing circuit a signal that corresponds to the reset signal.

31. The method of claim 30 including:

prior to storing the signal corresponding to the reset signal, clamping the second capacitive storage node to a voltage greater than the voltage corresponding to the reset signal; and

subsequently coupling the pixel readout line to the second storage node to store the signal corresponding to the reset signal on the second storage node.

32. The method of claim 26 including:

passing the pixel signal from the pixel readout line to an n-MOS source-follower;

clamping a capacitive storage node in a pixel signal processing circuit to a voltage less than the pixel signal appearing at an input to the n-MOS source-follower, wherein the storage node is clamped before passing the pixel signal through the n-MOS source-follower to the processing circuit; and

subsequently coupling an output of the n-MOS source-follower to the storage node in the processing circuit.

33. The method of claim 32 including:

resetting the pixel after storing the signal corresponding to the pixel signal in the processing circuit;

subsequently reading out a reset signal through the p-MOS

source-follower;

passing the reset signal through the n-MOS source-follower to the processing circuit; and

storing a signal corresponding to the reset signal in the processing circuit.

34. An imager comprising:

a pixel readout line;

an active pixel sensor including a p-MOS source-follower through which signals sensed by the sensor can be read out to the pixel readout line, a first switch that can be enabled to read out signals from the sensor, and a reset switch;

a signal processing circuit that can be coupled to the pixel readout line; and

a controller configured to provide control signals to cause the pixel readout line to be clamped to a voltage level greater than a voltage corresponding to a signal sensed by the sensor, and subsequently to cause the sensor signal to be read out through the p-MOS source-follower to the pixel readout line and to be stored by the processing circuit.

35. The imager of claim 34 wherein the processing circuit includes a capacitive storage node, and wherein the controller is configured to provide control signals to cause the capacitive storage node to be clamped to a voltage greater than a voltage corresponding to the sensor signal appearing on the pixel readout line, and subsequently to cause the pixel readout line to be coupled to the storage node.

36. The imager of claim 35 wherein the processing circuit includes a second capacitive storage node, and wherein the controller is configured to provide control signals to cause the reset switch in the pixel to be enabled, and subsequently to cause a reset signal to be read out onto the pixel readout line through the p-MOS source-follower, and to cause a signal

that corresponds to the reset signal to be stored on the second capacitive storage node.

37. An imager comprising:

a pixel readout line;

an active pixel sensor including a p-MOS source-follower through which signals sensed by the sensor can be read out to the pixel readout line, a first switch that can be enabled to read out signals from the sensor, and a reset switch;

a signal processing circuit;

an n-MOS source-follower having an output that can be coupled to the processing circuit; and

a controller configured to provide control signals to cause the pixel readout line to be clamped to a voltage level greater than a voltage corresponding to a signal sensed by the sensor, and subsequently to cause the sensor signal to be read out through the p-MOS source-follower to the pixel readout line and to be passed to the processing circuit through the n-MOS source-follower.

38. The imager of claim 37 wherein the controller is configured to provide a control signal to cause a capacitive storage node in the processing circuit to be clamped to a voltage less than the sensor signal at an input to the n-MOS source-follower, wherein the storage node is clamped before passing the sensor signal through the n-MOS source-follower to the processing circuit, and wherein the controller is configured to provide a control signal to cause an output of the n-MOS source-follower subsequently to be coupled to the storage node in the processing circuit.

39. The imager of claim 37 wherein the processing circuit includes a switch that is coupled to the storage node and that selectively can be closed to clamp the node to the voltage less than the sensor signal, and wherein the controller is

configured to provide a control signal to cause the switch in the processing circuit to be temporarily closed before causing the output of the n-MOS source-follower to be coupled to the storage node.

40. The imager of claim 37 wherein, when the output of the n-MOS source-follower is coupled to the storage node, the processing circuit stores a signal corresponding to the sensor signal, and wherein the controller is configured to provide control signals to cause the reset switch subsequently to be enabled, and to cause a reset signal to be read out from the sensor through the p-MOS source-follower and passed through the n-MOS source-follower to the processing circuit such that the processing circuit stores a signal corresponding to the reset signal.